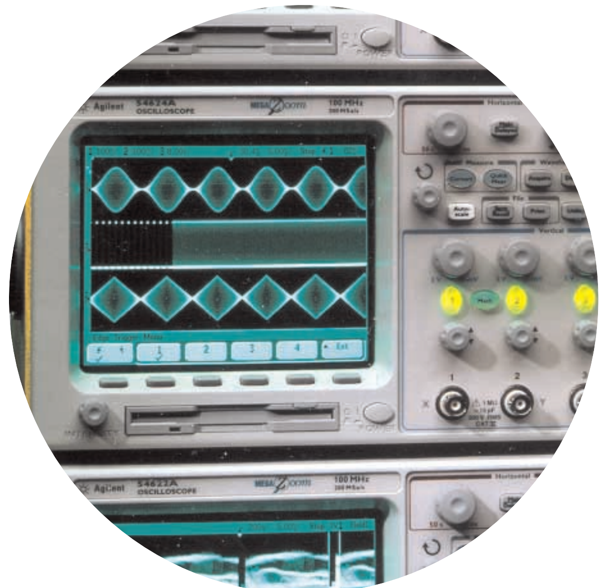
54622D

Agilent
I^2C Debugging

Application Note1351



With embedded systems shrinking, I^2C (Inter-integrated Circuit) protocol is being utilized as the communication channel of choice because it only needs two I/O lines for full implementation. However, with the benefit of using only two I/O lines comes the hassle of a complicated protocol. So, having a tool on the bench that eases I^2C troubleshooting is sure to add days to embedded engineers' life spans everywhere. The new Agilent Technologies 54622D oscilloscope adds a few more arrows to the embedded engineer's quiver of debugging tools. The 54622D extends the MSO (Mixed Signal Oscilloscope) line of test instruments which was started with the 54645D. It includes two analog channels and 16 digital channels, all of which can capture data at 200 MSamples/second and 400 Msamples/second, respectively. This is all fairly routine for anyone familiar with the 54645D; however the 54622D exceeds the earlier scope with its powerful trigger capabilities that are reminiscent of a logic analyzer.

Specifically, the 54622D offers a full suite of I^2C triggering capabilities. The I^2C connections to the 54622D are fully configurable. The SCL line and the SDA line can be assigned to any of the scope's 16 digital channels or to the two analog channels. In addition, there are six I^2C-specific triggers that are detailed below. Figure 1 shows the I^2C trigger menu on the 54622D. Figure 1 also shows how the I^2C lines can be configured to any channel – in this case the SCL line set on analog channel 1 and the SDA line set on analog channel 2.

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Start Condition: This triggers the scope anytime there is an I^2C start condition.

Stop Condition: This triggers the scope anytime there is an I^2C stop condition.

Frame(Start: Addr: Read: Ack: Data): The scope only triggers after the combination of start bit, control byte – configuring the slave to be read from, valid acknowledge, and then another byte. Both the control byte and the secondary byte can be set using the "Address" and the "Data" settings.

Frame(Start: Addr: Write: Ack: Data): This is the same as the previous trigger, except the slave must be configured to be written to.

Frame(Start: ~[Addr: Read: Ack: Data]): This trigger fires if any bit in the control byte, or the read bits, ack bits, or data bits do not match what is entered. This allows for triggering deep into an I^2C communication or to find spurious communication.

Frame(Start: ~[Addr: Write: Ack: Data]): This is the same as the previous trigger, except it looks for the absence of a write bit. this with two separate instruments!).

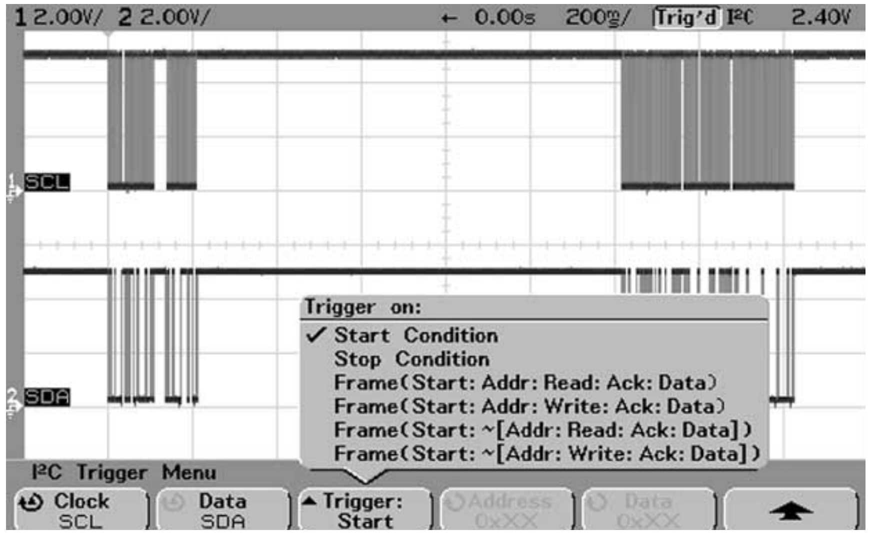

Figure 1. Shows the I^2C trigger menu

Both the stop and start condition triggers could also be accomplished using a pattern trigger, edge trigger, or the like, which is common on most DSOs. It is the other four triggers that really ease an embedded designer's task of troubleshooting an I^2C system.

For example, one common problem when using the I^2C bus is a master not receiving any communication back from a slave device on the I^2C bus. While this problem could be troubleshot with a standard DSO with a deep memory, the 54622D greatly speeds up the process. With a conventional DSO, the entire sequence must be captured and then zoomed-in and the individual transitions and data bytes must be analyzed one-by-one. This can become a tedious process in large systems with near-constant I^2C communication where individual triggering is nigh on impossible. With the new MSO, likely trouble spots are easily triggered on and analyzed.

For example, Figures 2 and 3 show a bad and good communication sequence between a master device and an I^2C temperature sensor. In this case, the temperature sensor was not sending information back to the master unit correctly. The 54622D was used to sift through a whole string of I^2C data to analyze just the temperature sensor data. Eventually the problem was narrowed down to the "Read Temperature" command sent to the temperature sensor. This was easily triggered on by using the "write" trigger – after the scope sees a start bit, control byte 48 (hex) configured to write (this is the temperature sensor's address), then data AA (hex) (the read temperature command), the scope triggers. After the trigger, the master should put the temperature sensor into read mode by sending a start bit and then a 48 (hex) control byte configured to read.

As shown in Figure 2, after the trigger the master sends the 48 (hex), unfortunately a start bit does not preface the 48 (hex), thereby causing the temperature sensor to ignore the command.

Figure 3 shows the correct sequence. After the master was configured to send the start bit correctly, the temperature sensor started sending the correct temperature.

With I^2C enjoying widespread industry support, debugging situations like the one described above are and will remain commonplace. The 54622D helps embedded engineers everywhere implement the bus with much less hassle.

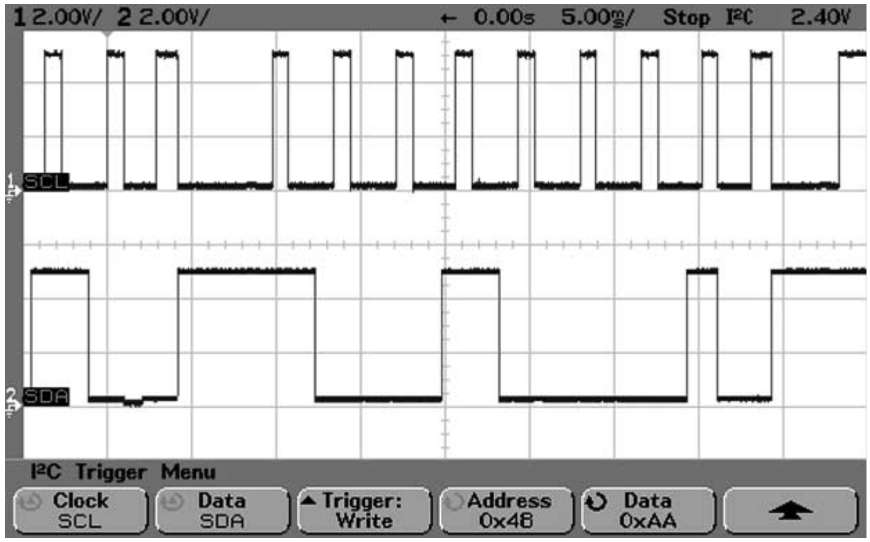

Figure 2. Shows a bad communication sequence

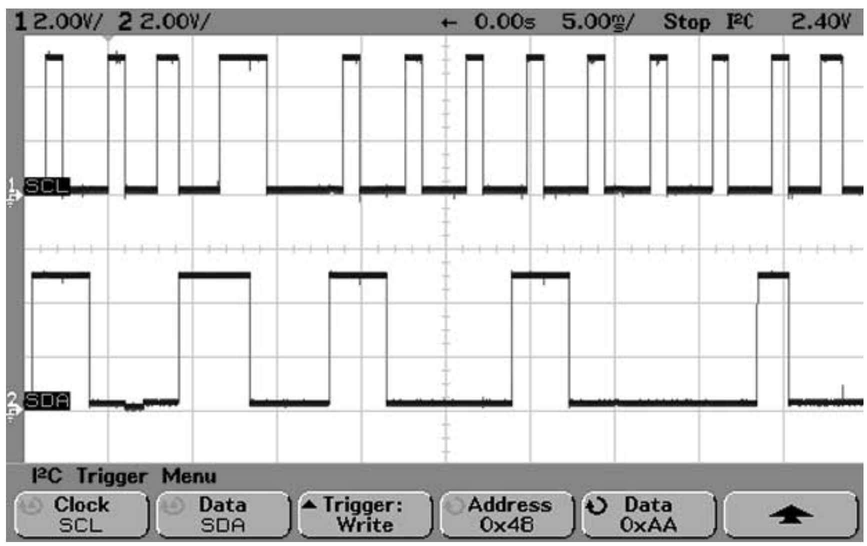

Figure 3. Shows the correct sequence

Figure 4. Five models to satisfy your bandwidth, channel count and budget needs

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